THE HP 85192B EEFet3 GaAs FET NONLINEAR MODEL† USED IN THE HIGH EFFICIENCY MICROWAVE POWER AMPLIFIER (HEMPA)

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Abstract

Most nonlinear circuit analysis programs that exist today were designed primarily for transient analysis. By incorporating more accurate models in simulation programs, accurate predictions of GaAs FET behavior can be accomplished. However, should the designer need to simulate GaAs FETs that operate at high DC-to-RF conversion efficiencies, a more sophisticated model is needed. A relevant and appropriate method is called harmonic-balance, as described by Quéré et al.

Introduction

Most nonlinear circuit analysis programs that exist today were designed primarily for transient analysis. By incorporating more accurate models in simulation programs, accurate predictions of GaAs FET behavior can be accomplished. However, should the designer need to simulate GaAs FETs that operate at high DC-to-RF conversion efficiencies, a more sophisticated model is needed. A relevant and appropriate method is called harmonic-balance, as described by Quéré et al. [1].

The HP EEFet3 model is an empirical model developed for fitting measured electrical behavior of GaAs FETs. The model includes the following features:

- An accurate isothermal drain-source current model that fits virtually all processes.
- Self-heating correction for the drain-source current.
- A charge model that accurately emulates measured capacitance values.

- A breakdown model that describes gate-drain current as a function of both V_{gs} and V_{ds}.
- A dispersion model that permits simultaneous fitting of high-frequency conductances and DC characteristics.
- The capability to extrapolate outside the measurement range used to extract the model.

jOmega Nonlinear HP EEFet3 Model

The software simulation package jOmega[2] includes a kernel routine for a GaAs FET nonlinear model. This kernel routine is a direct synthesis of the HP EEFet3 GaAs FET model. This GaAs FET kernel consists of time- and frequency-domain models.

By analyzing the nonlinear FET elements in the time domain, preservation of the physical characteristics of the elements can be accomplished. In the linear regime, the FET can be analyzed in the frequency domain by standard simulation techniques. The conversion between the time and frequency domains is accomplished using a Discrete Fourier Transform (DFT). The final HP EEFet3 model is shown in Figure 1.

For small-signal analysis, the HP EEFet3 model is altered to reflect a simplification of the simulation analysis, without significantly affecting the results of the analysis. From the large-signal model, the drain-channel capacitor is omitted with limited loss of accuracy. Two additional current sources, the drain-gate (I_{gd}) and gate-source (I_{gs}), are added. The drain-gate voltage controlled current source, Q_{gy}, represents the effect of avalanche current during large-signal operation. The gate-source current source, Q_{gc}, depicts the gate current that occurs when the gate-source junction is forward biased. The final current source, also depicted in the small-signal model, is the large-signal transconductance, I_{ds}.
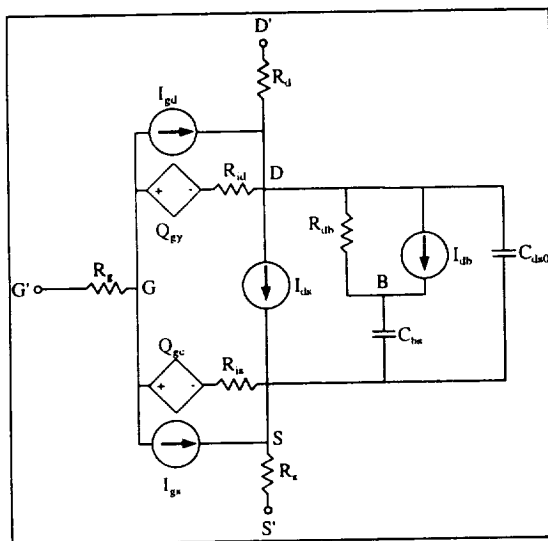

Figure 1—HP EEFet3 nonlinear GaAs FET model.

For brevity, only the NEC-9001-75, GaAs FET model and transistor will be discussed.

The high-frequency FET modeling software performs a series of DC- and S-Parameter measurements, based on predefined measurement configurations and on variables defined during the procedures. The measured values are then used to extract individual device parameters, through software conversion of the S-parameters to admittance or impedance parameters. The resulting model can be used to simulate the performance of the actual device in a circuit under design. The procedures involved use a series of setups to measure current or voltage vs. bias under different bias conditions. The purpose of the different measurement setups is to decouple the model equations, as much as possible, and effectively isolate the individual FET parameters. The equipment used for this study were the computer controlled HP4142B Modular DC Source/Monitor and the HP8753C S-Parameter Test Set, which is used to generate the operating linear S-parameters.

The first three measurements involve the device preview, used to verify proper device operation, and the device is operating within maximum voltage and current values. The measurements include I_g vs. V_{gs}, I_d vs. V_{gs} at V_{ds0}, and the I_d and V_{ds} vs. V_{gs}, more commonly known as the family of curves. These three measurements are used to obtain a set of measured DC I-V curves for the particular device for use in other measurement configurations. In the first measurement, the gate and drain voltages are monitored as the gate current is swept across the correct operating range. Figure 2 shows the bias arrangement for the Device-Under-Test (DUT).
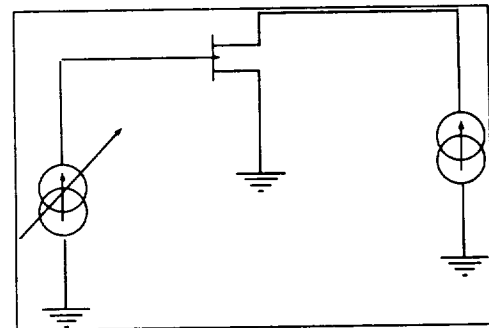

Figure 2—FET bias configuration.

The purpose of the setup is to use the gate current density of the device, and the gate width and length, to set the proper values for gate voltage.

The next DC procedure required to model the FET is to measure the drain current as a function of swept gate voltage, and is done at a single drain voltage bias point, or I_d vs. V_{gs} at V_{ds0}. Values of gate voltage are selected to take the device from pinch-off to I_{DSS}, drain saturation current, shown in Figure 3, and measures drain current as a function of swept gate voltage. Setting V_{ds0} appropriately helps to ensure that the rest of the I-V and dispersion parameters will extract correctly.
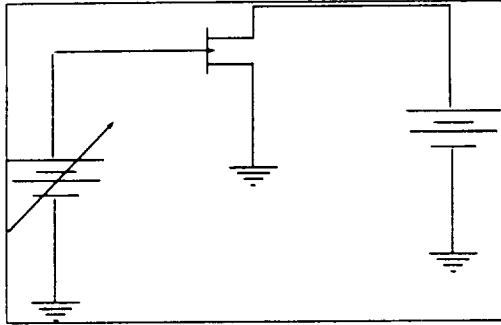
Figure 3—FET bias configuration for Id vs. Vgs at Vds0.

Figure 4 shows the results of the I_d vs. V_{gs} at V_{ds0} for the FET measured. From these initial values, the extraction of first order values for V_{g0} and V_{delt} is made.
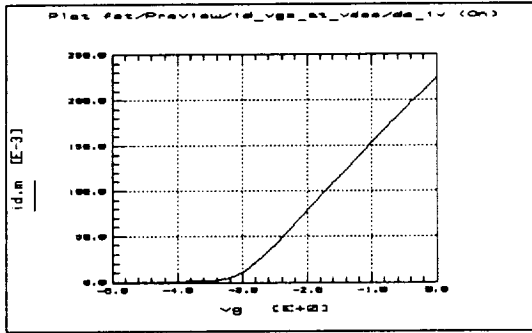

Figure 4—I_d vs. V_{gs} at V_{ds0} measured data for NEC-9001-75.

The next DC extraction required measurement of the drain current with respect to drain voltage, at several values of gate voltage. Shown in Figure 5.
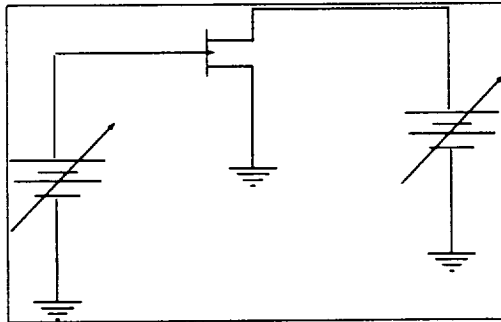

Figure 5—FET I_d for V_{ds} vs. V_{gs}.

Figure 6 shows the device pinch-off voltage increases as the higher drain voltage levels are reached. One early drawback of the HP EEFet3 model is that the nonlinear kernel uses a square law relationship for the pinch off region, which is not the case. Actual devices are
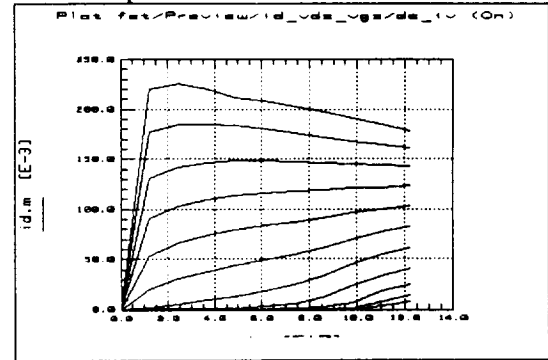
more accurately modeled by a quadratic relationship.

Figure 6—Measured I_d for V_{ds} vs. V_{gs}, NEC-9001-75.

A problem with the HP EEFet3 model is that a certain pinch off voltage may result that makes either the current or transconductance, but not both, zero. This is not the case in the quadratic model.

The next measurements are on the source, drain and gate resistances. There have been many papers written concerning the evaluation techniques to accurately determine these values. The most common is the end-resistance measurement. This is accomplished by using the unbiased drain as a voltage probe to measure the voltage at the top end of R_s while a substantial current is forced into the gate. However, this method has inaccuracies due to channel resistance effects. Another method, that overcomes this particular inaccuracy, is the Yang-Long Modified End Resistance Measurement Technique, and is used in the IC-CAP software package [3].

The authors of this technique provide derivations for the shift in V_{gs} that depend only on the gate diode's active resistance and R_s. The form of these expressions cannot be reduced to R_s=xx, so the measured and computed V_{gs} values are optimized until a suitable R_s is found [3].

In order for this method to work, the gate diode characteristics I_s and N, saturation current and ideality, respectively, must first be known. Thus, three measurements are required for this technique: the Yang-Long (preview), gate diode, and Yang-Long (measurement). The Yang-Long preview configuration is shown in Figure 5.

This procedure measures both I_g and I_d as a function of V_g and the results are displayed on a log scale, shown in Figure 7. The setup is used to ensure that the current input values chosen fall within the limits prescribed in the original paper by Yang and Long. [2]
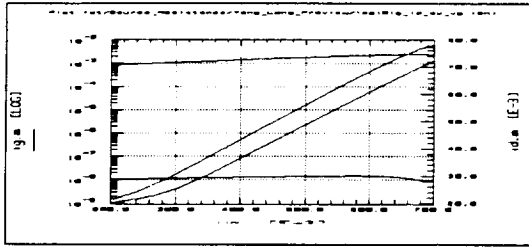
Figure 7—Yang-Long Preview measurement for the NEC-9001-75.

The dynamic resistance attributed to the gate diode formed by the Schottky contact is important to the extraction of all contact resistances. This procedure measures swept gate current as a function of gate voltage, with V_{ds} constant at zero, and displays the results on a log scale. These data are used for characterization of the gate diode forward conduction parameters I_s and N. The configuration is shown in Figure 3 and the results are shown in Figure 8.
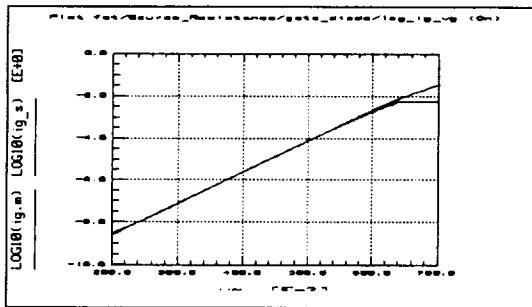
Figure 8—Gate diode measurement for the NEC-9001-75.

After verification of the preview measurements, the final Yang-Long measurement is completed. The Yang-Long configuration is shown in Figure 9 and the results are shown in Figure 10.
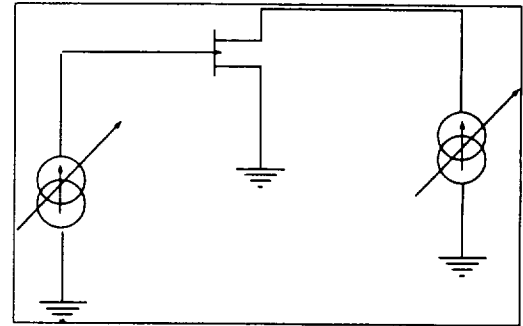

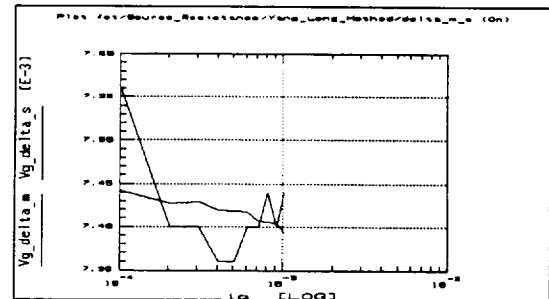**Figure 9—Yang-Long measurements method configuration.**

Figure 10—Yang-Long I_{gs} vs. V_{gs} measurement for the NEC-9001-75.

The next two setups perform the extraction for intrinsic and extrinsic parasitics from S-parameter data measured with a calibrated network analyzer. The method is similar to the work described by Dambrine, Cappy, Heliodore, and Playez [4].

The package resistance and inductance parasitics are extracted from S-parameter data measured across V_{gs} with V_{ds} at the nominal operating point. This setup is substantially the same as the work of Dambrine et. al., though it does not exactly track their work. The FET is forward-biased at three to five points. The extrinsic elements are constant, while the gate and channel characteristics change. Figure 3 shows the configuration of the R_g vs. R_d measurement and Figures 11 and 12 show the measurement results for each DUT.
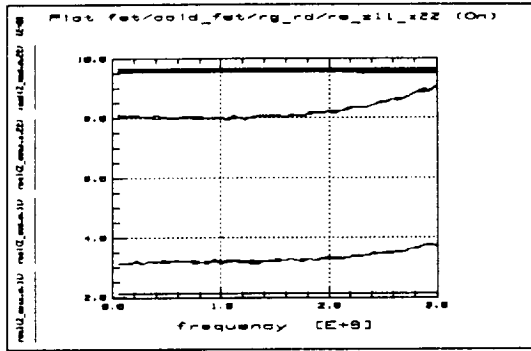
Figure 11—R_g, R_d vs. frequency real part measurement for the NEC-9001-75.
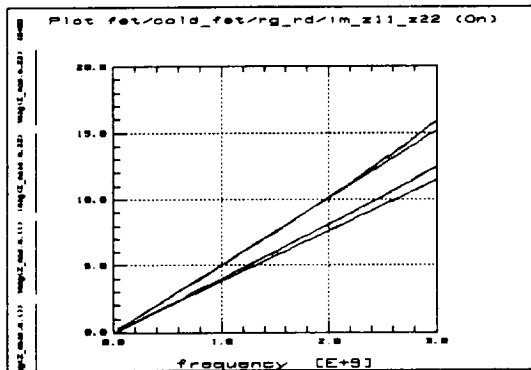

Figure 12—R_g, R_d vs. frequency imaginary measurement for the NEC-9001-75.

The method adopted here for approximating the package parasitics is derived from the work of Arnold et al. [5]. It requires only RF characterization at the device operating voltage and current points, and knowledge of the parasitic resistances. The technique has been used successfully applied to GaAs FETs and HEMTs.

To measure the package parasitics the DUT is configured as shown in Figure 3, and the results of those measurements are shown in Figure 13 through 15.
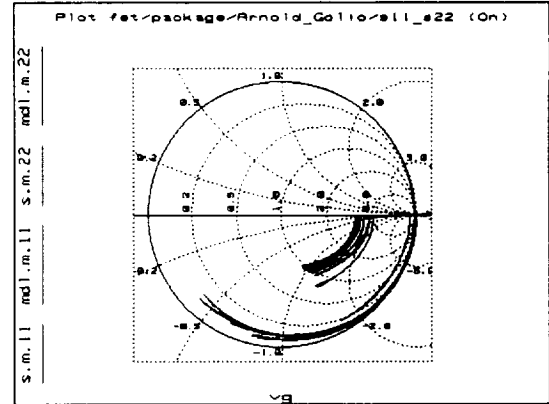

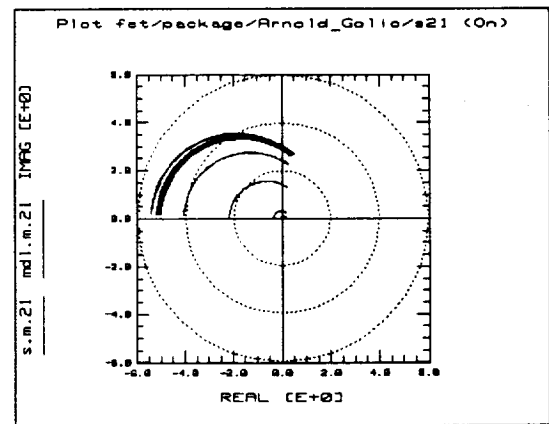Figure 13—S_{11} and S_{22} measured and simulated data for NEC-9001-75.

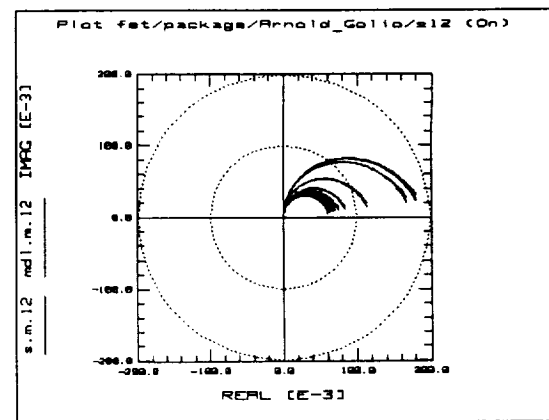Figure 14—S_{21} measured and simulated data for NEC-9001-75.

Figure 75—S_{12} measured and simulated data for NEC-9001-75.

The next area of DC extraction concerns the "ideality" of the FET. This ideality is a number that represents how well the FET mimics an ideal diode. This number should range from

1.0 (ideal diode) to about 1.5 to be acceptable, and the value is unitless.

The data from this DC measurement are used to extract the diode parameters V_{BI} (built in voltage), I_S (junction saturation current), and N (ideality factor). The results are shown in Figure 16.
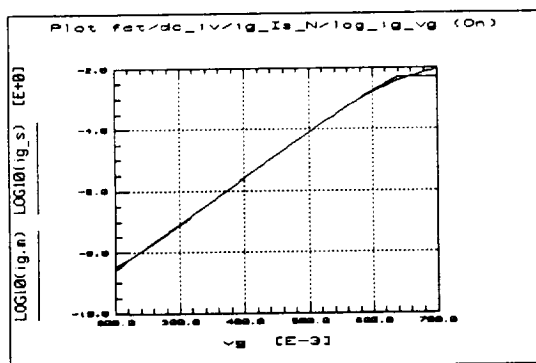

Figure 16—Measured Ideality curve, NEC-9001-75.

The bend at the high end of the curves defines where the parasitics start dominating and sets the bounds for extraction.

The next measurement for consideration is the refinement of I_{ds}-V_{gs} at V_{ds0}, which was made in the preview section and measures all the values of V_g with V_{ds} at a constant value of V_{ds0}. The configuration for the measurement is shown in Figure 3 and the measurement results are shown in Figure 17.
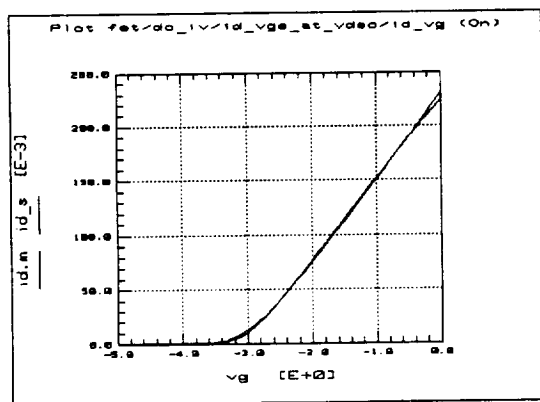

Figure 17—Measured I_{ds}-V_{gs} at V_{ds0}, NEC-9001-75.

The next measurement monitors the drain current with respect to drain voltage, at several values of gate voltage. The drain voltage is swept from 0 VDC to the upper limit of the DUT's operating range. Figure 3 shows the

proper configuration to measure the I_d vs. V_{gs}, and Figure 18 shows the typical results of these measurements.
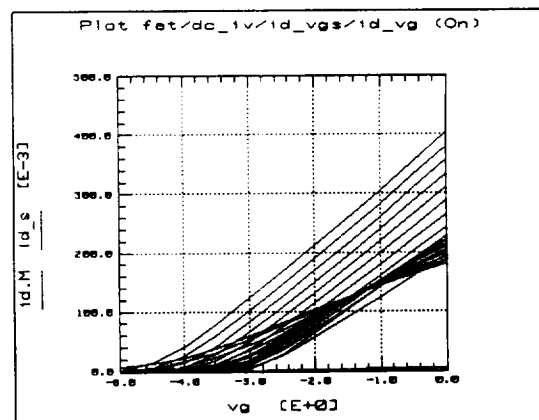

Figure 18—Measured I_d vs. V_{gs} NEC-9001-75.

Summary

Careful extraction of HP EEFet3 model parameters was found to yield models that gave reliable and predicted accurate results. As future refinement techniques emerge, better and more accurate models will be used. Finally, the simulated and measured S-parameters of the NEC-9001-75 model are shown in Figure 14.

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